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UNITED STATES PATENT APPLICATION

of

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for a

BUS HOLD CIRCUIT WITH POWER-DOWN AND OVER-VOLTAGE TOLERANCE

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to bus driver circuits and more particularly to bus hold circuits that maintain the output logic state when the source of the input signal assumes a high impedance state; and more particularly to CMOS bus hold circuitry that is over voltage tolerant, that does not create a leakage path when powered down, and is frugal of DC power and components.

Background Information:

Traditional bus hold circuits latch data from an input connection while providing a high impedance load on the input connection. Older bus hold circuits have neither power-down nor over-voltage tolerance and faulty or unacceptable conditions may occur under such circumstances. Over voltage will occur when, for example, a +5 volt logic system interfaces with a +3.3 V system, or transiently when severe input signal overshoots occur. Power down situations happen when a portion of a system is unpowered, say for maintenance purposes, or to conserve battery life. In such occurrences, leakage currents may unacceptably load the input signal. Such limitations are addressed by the present invention.

FIG. 1A illustrates one limitation of the prior art circuits. The circuit inverter output is connected back via an inverter, PMOS and NMOS, to latch and thereby hold the input data. But, from inspection when the input signal is driven from a +5V logic level

but the Vcc is +3.3V (or +1.8V) a leakage path exists through the drain to N-well diode, illustrated as D1. If the input voltage exceeds the Vcc, undesirable current will be drawn from the input signal connection and the latch circuit may malfunction. FIG. 1B shows the N-well to source leakage path in a sectioned view of a PMOS device, the leakage diode represented by D1.

Others have addressed some shortcomings of prior art bus hold circuits. U.S. patent no. 5,828,233 to Nguyen et al. (Nguyen) describes a circuit that provides both power-down and over-voltage protection tolerance. Nguyen employs passive components and two diode connected NMOS transistors arranged parallel anode to cathode, N3 and N4. Each of these diode connected transistors display about a 0.6V drop that have to be overcome before the circuit responds. Since the diodes are in parallel there is about a 1.2V zone (from one diode being on to the other diode being on) where the circuit operation is undetermined, ambiguous and asymmetrical. This 1.2V range is unacceptable. Asymmetrical is defined herein to mean that operation of the bus hold circuit displays markedly different delay/drive/noise level parameters under different input drive signals.

U.S. patent no. 6,097,229 to Hinterscher (Hinterscher) describes a circuit that is power-down tolerant but has no power-up or over-voltage tolerance.

U.S. patent no. 6,150,845 to Morrill (Morrill), which is commonly owned with the present application, describes a bus hold circuit with both power-down, over-voltage tolerance, and that prevents leakage from the input/output pins. But, the circuit undesirably contains many devices and consumes DC power in order to sense the over-voltage occurrence.

The Nguyen, Hinterscher and Morrill patents are each incorporated herein by reference.

It is an objective of the present invention to provide a bus hold circuit for use in computer, communications, interfacing and generally in virtually any digital system where symmetrical operation is desirable, and where such digital systems exhibit: power-down and over-voltage tolerance; economy of devices; and virtually no DC power consumption.

SUMMARY OF THE INVENTION

In view of the foregoing background discussion, the present invention provides a bus hold circuit, powered from Vcc, that addresses the limitations of the prior art.

The invention provides a CMOS inverter with a latching feedback inverter that includes a first PMOS device that selectively powers the second inverter. The N-well of this first PMOS device is connected to a pseudo power rail or prail. An arbiter circuit connects the more positive of the input voltage or the Vcc to the prail. This arrangement prevents the drain to N-well junction of this first PMOS device from becoming forward biased if Vin exceeds Vcc.

A comparator circuit provides a control signal of Vin, when Vin is at a higher potential than Vcc. The comparator circuit disconnects the control signal allowing it to float when Vcc is higher. When Vin is low, a second PMOS switch pulls the control signal low.

The N-wells of the PMOS devices in the bus hold circuit are connected to the prail provided by the arbiter circuit so that none of the PMOS devices will form a leakage path when Vin exceeds Vcc.

The comparator circuit, the first PMOS device, and the second PMOS switch acting together with the entire bus hold circuitry reduce the window of uncertainty between Vcc and Vin to about 100 millivolts.

It will be appreciated by those skilled in the art that although the following Detailed Description will proceed with reference being made to illustrative embodiments, the drawings, and methods of use, the present invention is not intended to be limited to these embodiments and methods of use. Rather, the present invention is of broad scope and is intended to be defined as only set forth in the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention description below refers to the accompanying drawings, of which:

FIG. 1A is; a circuit block diagram of prior art bus hold circuitry;

FIG. 1B is a simplified section of a PMOS showing the leakage diode;

FIG. 2 is a block diagram of an embodiment of the present invention; and

FIG. 3 is a more detailed schematic of FIG. 2;

FIGS. 4 and 5 are input current versus voltage trace comparing the prior art and the present invention;

FIG. 6 is an input current versus voltage trace comparing the prior art Nguyen circuit and the present invention.

DETAILED DESCRIPTION OF AN ILLUSTRATIVE EMBODIMENT

FIG. 2 in block form illustrates the approach of the present invention. In this circuit a separate power connection, referred to as a prail, is arranged to power part of the circuitry of the bus hold with the higher of Vin or Vcc as determined from the prail arbiter circuit 20 as discussed below. In this block diagram P3 connects Vcc to the latching inverter made up of N2 and P2. When Vin exceeds Vcc, P3 is turned off and prevents leakage current from flowing from Vin to Vcc as described with respect to FIG. 1A. Notice that the prail provides power only to the N-wells of the PMOS transistors which removes the leakage path from Vin to Vcc when Vin is larger than Vcc.

With respect to FIG. 2, three conditions are examined:

First, the "normal" condition when Vin is at a logic low. In this condition Vcc appears on the prail through the arbiter circuit 20; P4 is turned on driving the gate of P3 low turning it on. Vcc powers the feedback inverter comprising P2 and N2 via the source of P2. Under this condition, the comparator 24 is off and the OUT signal is "floating" or un-driven with respect to the comparator circuit (as discussed below). The inverter 28 output, Vout, 26 is high, N2 is on latching Vin low through R1. This latch preserves the data in the bus hold circuit in the case of the circuitry sourcing Vin assumes a high impedance condition. If Vin goes high, but still lower than Vcc and the PMOS thresholds, the inverter output 26 goes low turning on P2 and off N2. Vcc appears at the drain of P2

via P3 and latches the circuit high via R0 and R1. Again the latch information is preserved if the input enters the high-impedance state.

Second, consider that Vin now rises until Vin about equals but does not exceed Vcc. Prail remains at Vcc, the comparator remains off, P4 is off, but P3 remains on. P3 remains on because its gate was held low by P4, the OUT signal 22 remains a high impedance, and so there is nothing to provide charge to the P3 gate capacitance. P3 gate remains low maintaining P3 on and Vcc still powers the feedback inverter.

Third, consider Vin rising to exceed Vcc. In this condition Vin appears on the prail via the prail arbiter circuit 20. The comparator now turns on driving the OUT signal to Vin. Vin appears at P3's gate turning P3 off disconnecting the source of P2 from Vcc. But, importantly compared to the leakage path illustrated in FIG.1, the N-wells of the PMOS transistors are maintained at Vin levels such that no N-well to source junction is forward biased. In such a condition the leakage path will not exist. If Vcc goes to 0V, there will be no leakage path when a Vin signal (greater than 0V) appears.

FIG. 3 is a more detailed circuit schematic of FIG. 2. The arbiter circuit 20 of P8 and P9 drive the prail. N1 and P1 form the inverter 28, and P2, N2 form the feedback or latching inverter driving Vin via R0 and R1. Note that R0 and R1 are not needed for proper operation, but it has been found, that R0 and R1 act to make the operation of the bus hold buffer more symmetrical. The comparator circuit is shown in more detail. In the first conditions mentioned just above, when Vin is a logic low (less than Vcc) the comparator circuit 24 is off and the OUT signal is undriven (a high impedance) from the comparator. In such a condition, Vout is high and holds Vin low via the inverter P2/N2.

In the second condition mentioned above, when Vin rises to about equal to but not exceed Vcc, the comparator remains off and OUT is undriven. The Vout signal is low which turns on P2. P3 gate remains low, and Vin is pulled high to Vcc through R1, R0, P2 and P3.

Still referring to FIG. 3, in the third condition described above, where Vin is greater than Vcc, the comparator is described as being on where the drain of P6 and the gate of P3 are at Vin. Here P6 and P7 are on and will draw some small current via Vin to

charge the capacitance at the drain of P6 up to Vin. P4 is off , since its gate and source are both at Vin, and P3 is off since its gate is at Vin and its source is at the lower voltage Vcc. Vout goes low via N1, turning on P2. Since Vin is higher than Vcc, prail is at Vin and the N-well of P3 is at Vin, so the N-well diode of P2 is not turned on. In this case the drain of P3 will be driven to Vin via R1 and R0.

In the prail arbiter circuit 20, P8 and P9 have common signals on the gate of one and the source of the other, in a cross coupled manner. Notice that the N-well of each PMOS is connected to the drain. This will maintain the voltage at the drains via the source to N-well diodes of either PMOS at a diode drop maximum below the higher source voltage. But, if either Vcc or Vin is lower than the threshold of the relevant PMOS, P8 or P9, the higher of Vcc or Vin will be presented with no diode drop at the prail. Of note, is that there are no components that draw DC current from the prail. So, if the prail is at Vcc via P9, and P9 is turned off by Vin rising, prail remains at Vcc. Similarly if prail is at Vin via P8, it will remain there.

Still referring to FIG. 3, the comparator circuit 24 includes PMOS P5, P6, P7 and NMOS N3 and N4. When in the first and the second conditions above, the comparator is described as being off. In the first condition P4 is on holding the drain of P6 low, and the drain of P6 remains so after P4 is off. In the second condition, consider Vcc and Vin to be about equal. Here P5, P6, and P7 are all effectively open circuits drain to source, as are N4 and N5. This contrasts to the circuit in Morrill where the comparator always draws DC current. Morrill's M14 is always on as is M12, and an independent power supply V1 is provided. In the condition where Vin and Vcc are near each other, the arbiter circuit and comparator circuit act to reduce the window of uncertainty to about 100 millivolts. There is substantially less uncertainty than the 1.2 volts equivalent condition in the Nguyen invention. Note that this 100 millivolt range does not interfere with the proper action of the bus hold circuit itself, and once the Vin/Vcc differential exceeds this 100 millivolts the higher one will dominate the voltage levels in the circuit.

In any condition that Vin exceeds Vcc, for example if Vcc power is lost, Vin will appear at the prail via P8, the comparator is on and Vin will appear at the OUT terminal

via P7 and P6. In this condition Vin via the prail connects the N-wells of all the PMOS transistors (except inverter P1 PMOS where it is not needed) thereby preventing the N-well to sources of these PMOS transistors from providing a leakage path from Vin to Vcc

FIG. 4 compares Iin/Vin traces 42 and 44 for the circuits in FIG. 1 and FIG. 3, respectively, with Vcc set to +3.0 V. Notice that when Vin exceeds Vcc 40, the Iin 42 for the circuit of FIG. 1 continues to rise, due to the leakage path discussed above, while Iin 44 remains substantially at 0.00A for the inventive circuit of FIG. 3.

FIG. 5 compares Iin and Vin for the same circuits with Vcc at 0.0V. Here when Vin exceed the MOS threshold of about 0.5V the circuit in FIG. 1 draws current 52 (again via the leakage path discussed above) while the circuit of FIG. 3 draws none 54.

FIG. 6 compares Iin and Vin for the circuit of Nguyen 60 and the inventive circuit 62 with Vcc at +1.8V. The Nguyen circuit does not exhibit the leakage path of the circuit in FIG. 1. However, when Vin approaches within about 0.5V of Vcc, Iin 60 approaches zero 64. This is the zone where Nguyen's circuit loses its drive, due to the diodes discussed above, and exhibits unacceptable asymmetrical input/output behavior. The inventive circuit shows no such characteristic and operates well up through to where Vin exceeds Vcc 66. Also, notice the symmetry of the inventive circuit curve 62 traversing from Vin from 0 to 1.8V compared to the unsymmetry 60 of Nguyen circuit.

It should be understood that above-described embodiments are being presented herein as examples and that many variations and alternatives thereof are possible. Accordingly, the present invention should be viewed broadly as being defined only as set forth in the hereinafter appended claims.

What is claimed is: